REMARKS

Claims 1-3, 5-7, 9-11, and 13-15 were rejected under 35 U.S.C. 102(e) as being anticipated by Hagihara.

Applicant appreciates the indication that claims 4, 8, 12 and 16 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 4, 8, 12 and 16 were rewritten in independent form to include the limitations of the base claims and any intervening claims. As such claims 4, 8, 12, and 16 are now allowable.

With regard to claims 1, 5, 9, and 13 the examiner has stated that it is inherent that the transistors in the logic circuit are series connected. Applicant argues that there is no inherency in the box representation of a logic circuit in the Hagihara patent. Claim 1 of the instant invention requires that at least one of the MOS transistors connected in series be NMOS and at least one of the series MOS transistors be PMOS. In describing the so called inherency of the logic block diagram the examiner has not described the requirement of claim 1 that at least one of the series MOS transistors be NMOS and one be PMOS. As such this requirement cannot be found in the Hagihara patent and claim 1 and its dependent claims are allowable over the Hagihara patent.

Claims 9 and 13 require a parallel connection of the MOS transistors. In response to applicants request that the examiner describe with particularity what was meant by inherency, the examiner has described in underlined bold type an inherency of series connected transistors. Although applicants argue that no such inherency exists, under the examiners position the inherency is a series connection. Therefore the parallel connection required in claims 9 and 13 are not inherent in the Hagihara patent and claims 9 and 13 are allowable over the cited art. In addition all dependent claims that depend on claims 9 and 13 are also allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with Markings to Show Changes Made."**

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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Version with Markings to Show Changes Made

4 (Amended). A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected MOS transistors wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor, at least one of said plurality of series connected MOS transistors is a PMOS transistor, and [The dynamic logic circuit of claim 1 wherein] at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body[.] ;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

8 (Amended). A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected PMOS transistors [The dynamic logic circuit of claim 5] wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body[.] ;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

12 (Amended). A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor, at least one of said plurality of parallel connected MOS transistors is a PMOS transistor, and [The static logic circuit of claim 9 wherein] at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body[.] ;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node which is connected to said first common node of said pull-down network.

16 (Amended). A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected PMOS transistors with a first and second common node [The static logic circuit of claim 13] wherein at least one of said PMOS transistors in said pull-down network has a gate tied to a floating substrate body[.] ;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node connected to said first common node of said pull-down network.